UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,579	03/01/2004	Peter W. Lee	AP99-005BB	9866

7590 05/17/2006

George O. Saile
28 Davis Avenue
Poughkeepsie, NY 12603

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/790,579	LEE ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed April 28, 2006 has been entered. Claim 13 has been amended. Claims 13-15 are pending.

Drawings

2. The drawings, FIG. 3a and 3b were received on April 28, 2006. These drawings are acceptable.

Specification

3. The disclosure is objected to because of the following informalities:

As amended beginning on page 11, last two lines to page 12, line 3: The split gate cells 50, 51, 52, 53 in each column have the same orientation such that the portion of the **channel 54** under the stacked gate of a cell 50 is connected to a bit line BL and the portion of the **channel 55** under the select/control gate of the cell 50 is connected to a source line SL. In the adjacent column the portion of the **channel 56** under the staked gate of the cell 51 is connected to a source line SL with the bit line BL connected to the portion 57 of the channel under the select/control gate.

"54"; "55" and "56" are not channels, they are just the portions of the channel under the gate stacked.

Therefore, the correction should be: -- The split gate cells 50, 51, 52, 53 in each column have the same orientation such that the portion **54** of the channel under the stacked gate of a cell 50 is connected to a bit line BL and the portion **55** of the channel under the select/control gate of

the cell 50 is connected to a source line SL. In the adjacent column the portion **56** of the channel under the staked gate of the cell 51 is connected to a source line SL with the bit line BL connected to the portion 57 of the channel under the select/control gate.

As amended page 12, beginning on line 21: In Fig. 3b the portion of the channel under the stacked gate of each cell 54 is connected to bit line BL, and the portion of the channel under the select/control gate of each cell 55 is connected to a source line SL.

"54" and "55" are not the cells, they are portions of the channel under the cell **50**.

Therefore, the correction should be: -- In FIG. 3b the portion **54** of the channel under the stacked gate of each cell **50** is connected to bit line BL, and the portion **55** of the channel under the select/control gate of each cell **50** is connected to a source line SL.--

Appropriate correction is required.

Claim Objections

4. Claim 13 is objected to because of the following informalities:

Lines and 17 recite: select and control gate.

However, the specification discloses: "select/control gate".

Page 9, lines 7-8 defines the transistor as follows: "The split gate flash memory cell 41 transistor has a portion of its channel under a stacked gate configuration **where the control gate and the floating gate are stacked together** and is called the "memory transistor". The other

portion of the channel of the split gate flash memory cell 41 transistor is below only the control gate and is called "the select transistor".

Therefore, the phrase "stacked gate" is referring to control gate stacked above the floating gate combined.

The phrase "select/control gate" means select or control gate. These two terms "select"; "control" should not be used together with "and" in the same phrase to create a confusion.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13, step c) recites: "cell layout in a first column of cells having a same cell layout in adjacent second and a third columns of cells, whereby a first bit line connects to a portion of a channel under a select/control gate a memory device of the cells in the first column and a second bit line connects to the portion of the channel under the gate stacked of the third column of cells".

Since the layout of the cells are the same for all cells in first, second and third columns, then the bit line should connect to the same portion of any cells in the first and third columns.

The specification already discloses that portion 54 of the cell 50 under the gate stacked bit line is connected to first bit line, then the same portion 54 of the cell 52 under the gate stacked should connect to second bit line.

The claim on the other hand claimed the reverse, thus contradicting the previous limitation, which is layout of the cell are the same.

Claim 13, step d) recites: "**said bit line** extends full length of **said columns**, laying between said cells of said first and third columns,".

However, in step c), there are two bit lines, first and second bit lines, and three columns of cells, first second and third columns of cells.

It is not known which of the "said bit line" and "said columns" the claim are referring to.

Claim 13, step e) also contradicting the "same layout" as claimed in step c).

Therefore, claim 13 is indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kuroda et al. (U.S. Patent No. 5,548,146).

With respect to claim 13, as best understood by the examiner, Kuroda teaches a non volatile memory as claimed including:

a) flash memory cells (Q) organized in rows (Q00, Q01, Q02) and columns (Q00, Q10, Q20),

b) cells (Q) in a row are interconnected by a word line (W) connecting to control gates of the flash memory cells (Q) in the row,

c) cell (Q02) layout in a first column of cells (Q02, Q12, Q22) having a same cell layout in adjacent second (Q01) and a third (Q00) columns of cells, whereby a first bit line (D3) connects to a portion (right) of a channel under a stacked gate a memory device of the cells (Q02, Q12, Q22) in the first column and a second bit line (D1) connects to the portion (right) of the channel under a stacked gate of the third column of cells (Q00),

d) the bit line (D3) extends full length of the columns (vertically), laying between the cells of the first (Q02) and third (Q00) columns,

e) a source line (D2) extends full length of columns (vertically), laying between the cells of the first (Q02) and second (Q01) columns, whereby the source line (D2) connects to the portion (right) of the channel under the stacked gate of the second column of cells (Q01) and the source line (D2) connects to the portion (left) of the channel under the a select/control gate of the first column of cells (Q02),

f) the flash memory cells (Q) organized by a vertical page comprising the memory cells in the first column (Q02), inherently, to perform a program operation, whereby a source line voltage and a bit line voltage of the vertical page are set for the program operation and a word line program voltage is stepped from cell to cell in the first column,

g) the flash memory cells (Q) organized by horizontal block comprising a first row of cells (Q02) adjacent to a second row of cells (Q12) and whereby all bit lines, source lines and word lines of the horizontal block are coupled to a same low voltage and then word lines coupled to cells in the horizontal block are biased to an erase voltage, inherent of the erasing operation,

h) the cell (Q) layout in the columns allowing vertical page programming and horizontal page/block erase. (See Fig. 5).

With respect to claim 14, the bit lines (D3) of Kuroda provide a path to read data stored in the cells (Q) when performing a read operation.

With respect to claim 15, the source line (D2) connect to sources of cells (Q02, Q12, Q22) of the first column, connect to drains of cells (Q01, Q11, Q21) of the second column and connect to source voltages.

Response to Arguments

7. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER